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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,266	05/20/2004	Dominik J. Schmidt	IVT.0033US	4584

21906 7590 03/24/2008

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EXAMINER	
PHAN, DEAN	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
03/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,266	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	DEAN PHAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/06/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim(s) 1 is objected to because of the following informalities:

In claim 1, "a host processor and configured to execute" in line 2 should be changed to "a host processor configured to execute". Appropriate correction is required.

Response to Arguments

Applicant's arguments with respect to claims 20-40 have been considered but are moot in view of the new ground(s) of rejection. (*See below Office Action for detail*)

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 22 and 35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, *"selectably configure the second portion of the plurality of processors to execute instructions belonging to an instruction set of the first processor family subsequent to the second portion of the plurality of processors processing instructions belonging to an instruction set of the second processor family"*, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed

invention. There is nowhere in the specification discloses how a plurality of processors in the second portion which is firstly configured to execute instructions belonging to second processor family has ability to configure to process instructions belonging to the first processor family. For the purpose of examination, Examiner treats the limitation as "selectably configure the first portion of the plurality of processors to execute instructions belonging to an instruction set of the first processor family subsequent to the second portion of the plurality of processors processing instructions belonging to an instruction set of the second processor family". Correction/Clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 23-33, 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt (U.S 7142882) in view of Applicant Admitted Prior Art (hereafter APA).

As to claim 20, Schmidt discloses a wireless communication device (Fig. 1) comprising:

a processor (fig. 1 one of MIPS processor in Wireless COMM 100) configured to execute instructions belonging to an instruction set of a first processor family (col 7 lns 1-10; MIPS family); and

a reconfigurable processor core (fig. 1 Wireless COMM 100) coupled to the host processor (fig 2; *The wireless Comm 100 is coupled to any MIPS processor*), wherein the reconfigurable processor core includes a plurality of processors (fig. 2 CPU, DSP, ASIC), wherein portions of the plurality of processors are selectably configurable to execute instructions belonging to a plurality of instruction sets (col 3 lns 50-col 67; e.g. *discrete cosine transfoms or Viterbi encodings, among others*);

wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of the first processor family (col 3 ln 50-col 4 ln 25; *The other MIPS processors are in a first portion*);

wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family (DSP or ASIC processor family); and

wherein said processor and the reconfigurable processor core are both located on a single integrated circuit die (col 3 lns 38-45).

Schmidt does not disclose said processor is a host processor. However, in the same field of art, APA discloses that it is known to provide processing systems having one or more central processing units, a memory and a host processor, such as the ARM processors or MIPS processors. The central processing units execute dedicated code such as signal processing code, while the host processor coordinates the central

processing units and interfaces with an external system (par. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement a host processor in order to improve the performance and to take advantage of commercially available off the shelf system. (*see par. 2*).

As to claim 23, all limitations are in claim 20, further comprising a plurality of digital signal processors configured to execute instructions corresponding to one or more embedded functions (col 7 lns 50-67).

As to claim 24, all limitations are in claim 20 but does not disclose the second portion of the plurality of processors collectively forms a second host processor. However, using two or more processors instead of a single one to handle and share a particular function is common in the art at the time of invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to collectively forms the second portion of plurality of processors as a second host processor in order to avoid bottleneck problems, to improve the host performance and the stability of the device.

As to claim 25, all limitations are in claim 20, further comprising an analog circuit portion located on the integrated circuit (fig. 1 elements 110, 130, 111…) and coupled to a digital circuit portion (elements 150, 170, 190) that includes the host processor and the reconfigurable processor core, wherein the analog circuit portion includes:

a cellular radio core (element 110) configured to provide two-way communication via one or more wireless channels (col 4 ln 56-col 5 ln 20;

a radio sniffer coupled to the cellular radio core (element 111); and

a short-range wireless transceiver core coupled to the cellular radio core (element 130) and configured to provide two-way communication via one or more short-range wireless channels (col 5 lns 36-45).

As to claims 26-30, all limitations are in claim 25, wherein the reconfigurable processor core is coupled to the cellular radio core (fig. 1), and configured to process instructions corresponding to a plurality of wireless radio communication protocols includes a Bluetooth TM or IEEE802.11 protocol (col 4 ln 56-col 5 ln 2).

As to claim 31, all limitations are in claim 25, further comprising a router (elements 190) coupled to the host processor (col 1 lns 60-67), the cellular radio core (element 110), and the short-range wireless transceiver core (element 130), wherein the router is configured to track destinations of packets and to send the packets in a parallel through a plurality of separate wireless communication channels (col 6 lns 45-55).

As to claim 32, all limitations are in claim 31, wherein the router is further configured to determine which of the plurality of separate wireless communication channels provides an optimum transmission medium, and to send the packets in a parallel in response to determining that more than one or more channels is less than optimum (col 4 lns 40-55).

As to claims 33, 36-39, all same elements of Claims 1, 26-28, 31-32 are listed, but in device form rather than method form. Therefore, the supporting rationale of the rejection to Claims 1, 26-28, 31-32 applies equally as well to Claims 33, 36-39.

As to claim 40, all same limitations are in claim 1 with further: a system host processor (Fig. 2 CPU 220);

Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt in view of APA and further in view of Stravers (WO 03/005225).

As to claim 21, Schmidt discloses the device as recited in claim 20, does not explicitly disclose a processor type select circuit configured to selectably configure the reconfigurable processor core to process instructions belonging to either an instruction set of the first processor family or an instruction set of the second processor family. However, in the same field of art, Stravers discloses a plurality of processors from plurality of processor type families (fig. 1-2 ARM, MIPS, REAL, DSP…) and a processor type select circuit (circuits 3 & 6). The processor type select circuit is configured to select a processor type to process instructions belonging to either an instruction set of the first processor family or an instruction set of the second processor family the processor type (abstract). Therefore, it would have been obvious for one of ordinary skill in the art at the time of inventions to implement the teaching of Stravers into Schmidt's invention, by configuring a processor type select circuit to selectably configure the reconfigurable processor core to process instructions belonging to either an instruction set of the first processor family or an instruction set of the second processor family ARM processor families into the reconfigurable core in order to improve performance of the processor, to provide wide applicability and cost effective implementation of an IC (page 1).

As to claim 22, Schmidt and Stravers disclose the device as recited in claim 21 further: processor type select circuit configured to selectably configure the first portion of

the plurality of processors to execute instructions belonging to an instruction set of the first processor family subsequent to the second portion of the plurality of processors processing instructions belonging to an instruction set of the second processor family (page 5 lns 5-15).

As to claims 34-35, all same elements of Claims 2-3 are listed, but in device form rather than method form. Therefore, the supporting rationale of the rejection to Claims 2-3 applies equally as well to Claims 34-35.

Examiner's note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEAN PHAN whose telephone number is (571)270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272 4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

dp

/Ilwoo Park/

Primary Examiner, Art Unit 2182